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LETTERS TO THE EDITOR

OPERATIVE DEFINITION OF THE THRESHOLD OF TUNNEL DIODE SWITCHING CIRCUITS*

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The threshold of a tunnel-diode circuit depends on the rise-time of the triggering pulse and as a consequence on all the reactive parameters of the actual circuit. In this letter we give the first results of the threshold variation vs input pulse rise-times. Furthermore our purpose is, to suggest an operative definition of the dynamic threshold of the circuit that should be applied to input pulses ranging from infinite (d.c. level) to zero (the step) rise-time.

We recall that the steady-state circuit threshold is the value of the input d.c. signal causing the tunnel-diode to regenerate with an infinite time (see appendix).

We take as a general regenerative condition the following (fig. 1b):

$$\mathrm{d}(i_L+I_{in})/\mathrm{d}V = \mathrm{d}f(V)/\mathrm{d}V. \qquad (1)$$

The current $C\mathrm{d}V/\mathrm{d}t$ (fig. 1b) is not necessary equal to zero[1]), but has a minimum. It is zero for the static threshold in which case the triggering time delay is infinite.

The above condition on the charge current of the capacitance has the following analytical expression:

$$\mathrm{d}^2V/\mathrm{d}t^2 = 0 \quad \text{and} \quad \mathrm{d}^3V/\mathrm{d}t^3 > 0,$$

which is another definition of the regenerative point.

In the case of finite (or zero) input pulse rise-time, often[2]) the dynamics threshold is referred to what we have already done for the steady state. This may be correct if we relate the definition to the tunnel-diode itself without reactive elements neither intrinsic (self-inductance) nor external[3]) in which case steady state and dynamic threshold have the same value. In fact, if we have an inductance in the circuit even if its value is very low, we cannot assume an infinite switching delay time, for we will exclude any contribution due to the inductance.

We will thus define the dynamic threshold of the

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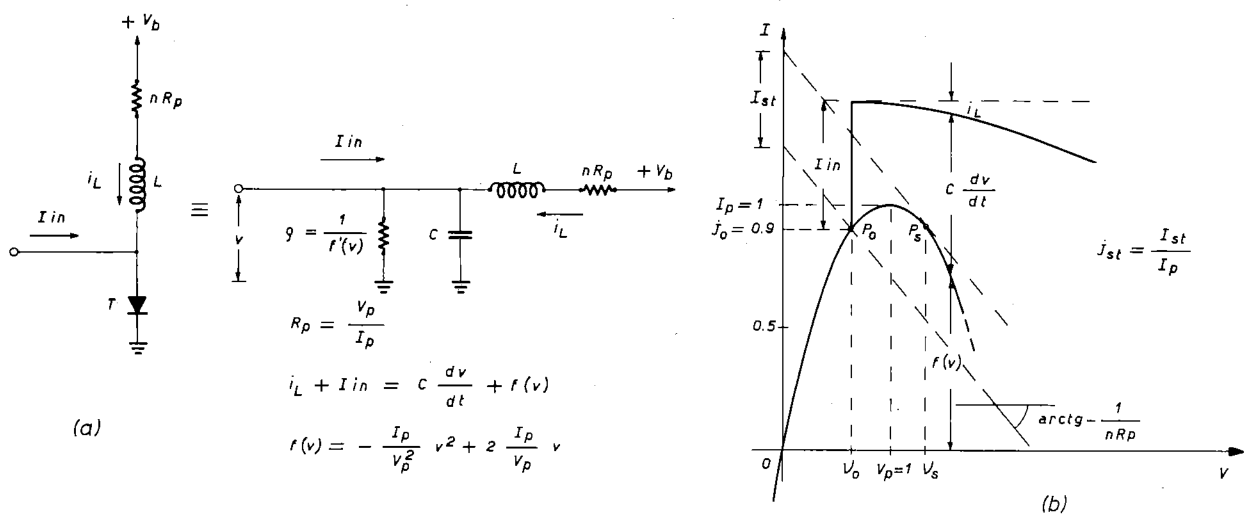


Fig. 1. Tunnel-diode monostable circuit. (a) equivalent circuit and differential equations, (b) graphical characteristics and symbols representation.

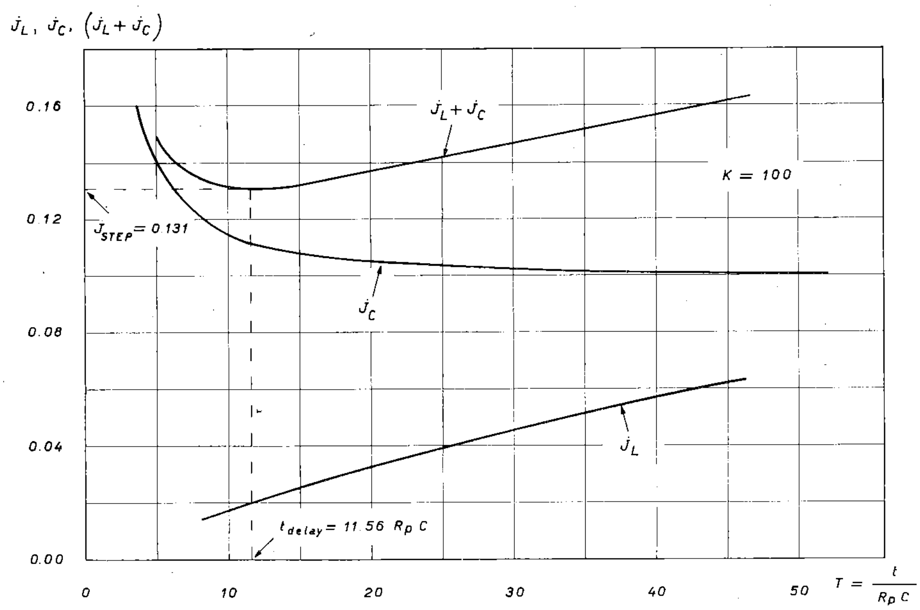
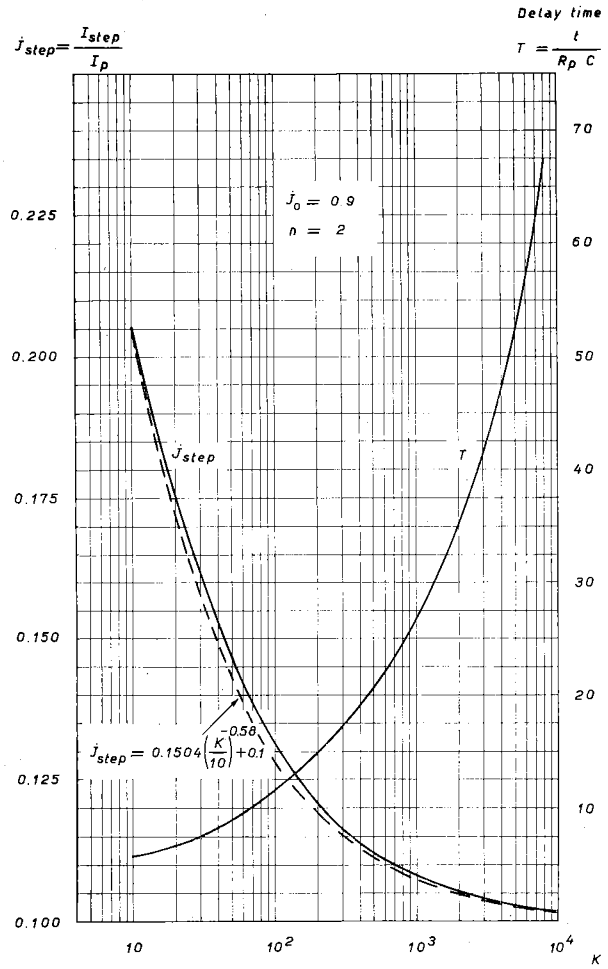


Fig. 2. Graphical representation of the variation of the normalized current in the inductance j_L and of $j_c = Q + 1 - j_0$ (j_0 = input current). The sum $j_L + j_c$ presents a marked minimum.



circuit: "The amplitude of the input signal for which the condition (1) is satisfied when the sum of the current in the capacitor and in the inductance j_s has a minimum."

To explain this, let us think of a triggering step pulse with infinite overdrive* applied to the circuit. This will produce an output with zero delay-time. Let us decrease the overdrive: the delay will increase. To a definite value of the overdrive and delay the condition (1) is satsfied with the minimum of j_s as a function of the overdrive.

Trying to find tentatively the threshold with the help of a digital computer (step input pulse for $K = 10^2$), with that criterium the value of the triggering delay time has been found about 9 R_pC, corresponding to a threshold calculated with a relative incertitude $\leq 10^{-3}$.

Let us now compute analytically the value of the threshold when the input pulse is a step. This may be done with this approximated procedure:

The delay time as a function of the overdrive is[4])

$$t/(R_pC) = T = Q^{-\frac{1}{2}} \tan^{-1} \{(1 - v_0) Q^{-\frac{1}{2}}\}.$$

* Overdrive is defined as:

$$Q = (I_{in} + I_0 - I_p)/I_p = j_{in} + j_0 - 1 .$$

Fig. 3. Threshold values for the input step and corresponding delay-times vs K, for $n = 2$.

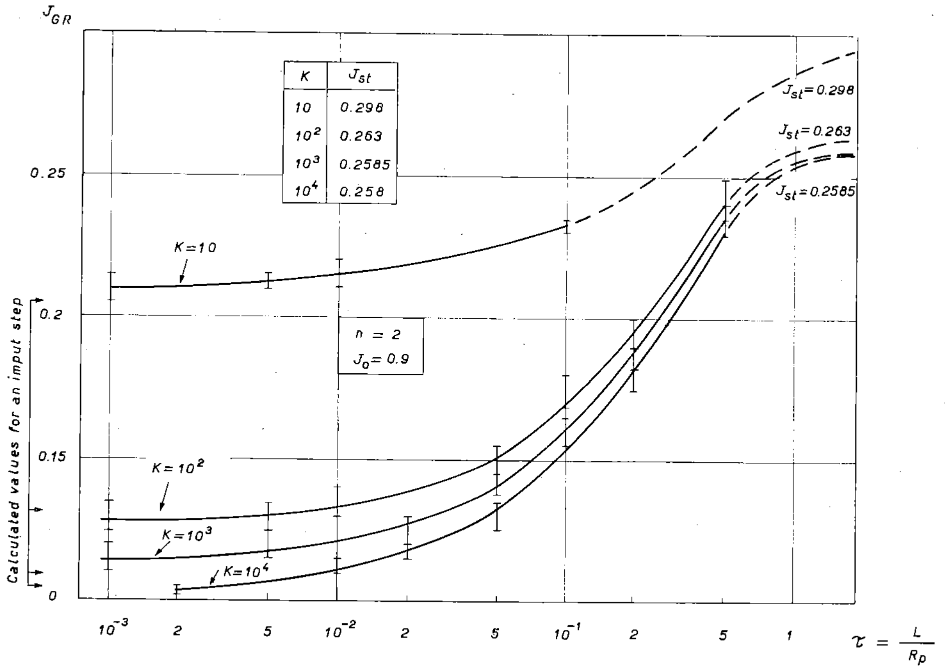


Fig. 4. Threshold values obtained from the numerical integration of the differential equations for exponential input with time constants ranging from 10^{-3} L/R_p to 5×10^{-1} L/R_p, with the input final values between 10^{-2} I_p and 10^{-3} I_p.

Now, the normalized current variation in the inductance, for an exponential voltage input pulse of rise-time T

$$v = (1 - v_0)\left\{1 - \exp\left(-\frac{2.2}{T}\frac{t}{R_p C}\right)\right\}$$

can be written as:

$$j_L = \left(\frac{1-v_0}{n}\right)\left[1 + \frac{nT}{2.2K - nT}\,e^{-2.2} - \right.$$
$$\left. - \frac{2.2K}{2.2K - nT}\exp(-nT/K)\right].$$

The sum of the two currents $j_c = Q + 1 - j_0$ and j_L vs time T has a minimum whose value j_{step} we define as the threshold (fig. 2).

In this way we have obtained once more the threshold value related to definite time delays.

The threshold values for the input step and corresponding characteristic delay-times vs K and for $n = 2$ are shown in fig. 3.

The numerical integration of the differential equations give for the threshold the values shown in fig. 4. They are for exponential input, with time constants τ ranging from 10^{-3} L/R_p to 5×10^{-1} L/R_p while the final values of the input have incertitudes between 10^{-2} I_p and 10^{-3} I_p.

As can be seen (fig. 4), the points calculated for an input step with the procedure mentioned above, are in good agreement with those we may extrapolate, for zero rise time, from the values obtained with the digital computer. The values of the steady state thresholds are also indicated for different values of K.

It is obvious that the analytical approximated procedure can be extended, with some increase in the complexity of the calculation, to the cases in which input rise-times are different from zero.

We verified that the dependence of j_{step} from K may be expressed (for K values from 10 to ∞) as (fig. 3):

$$j_{step} = 0.1504(\tfrac{1}{10}K)^{-0.58} + 0.1.$$

Further calculations are in progress and more complete results will be published later.

Appendix: The value of the steady-state circuit threshold is theoretically obtained as follows: The analysis of the differential equations of the circuit of fig. 1a leads to the following stability conditions[5]):

$$nR_pC + Lf'(V) > 0,$$
$$1 + nR_pf'(V) > 0,$$

where

$$R_p = V_p/I_p; \qquad \rho = 1/f'(V),$$

while[4])

$$f(V) = (-I_p/V_p^2)V^2 + (2I_p/V_p)V$$

is the normalized equation for the tunnel-diode characteristic in the region near the peak.

These conditions define two points on the portion with negative resistence of the tunnel-diode characteristic as limits between the stable and the instable region. The instable region is on the right of the point nearer to the peak. This point is defined as:

$$P_s = \{v_1, f(v_1)\} \quad \text{for} \quad n < \sqrt{K}$$
$$P_s = \{v_2, f(v_2)\} \quad \text{for} \quad n > \sqrt{K}$$

where

$$v_1 = V_p \{(n/2K)+1\}$$
$$v_2 = V_p \{(1/2n)+1\}$$

with $K = L/(R_p^2 C)$ as the characteristic parameter of the circuit.

The steady state threshold is obtained evaluating the intercepted segment on the I-axis by the two straight lines of angular coefficient $-1/(nR_p)$ drawn through the bias point P_0 and through P_s (fig. 1b). We obtain, normalizing to I_p, V_p

$$j_{st} = \frac{1}{2K} + \frac{1}{n}(1-v_0) - \frac{n^2}{4K^2} - j_0 + 1 \quad \text{for } n < \sqrt{K},$$

$$j_{st} = \frac{1}{n}(1-v_0) - \frac{1}{4n^2} - j_0 + 1 \qquad \text{for } n > \sqrt{K}.$$

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